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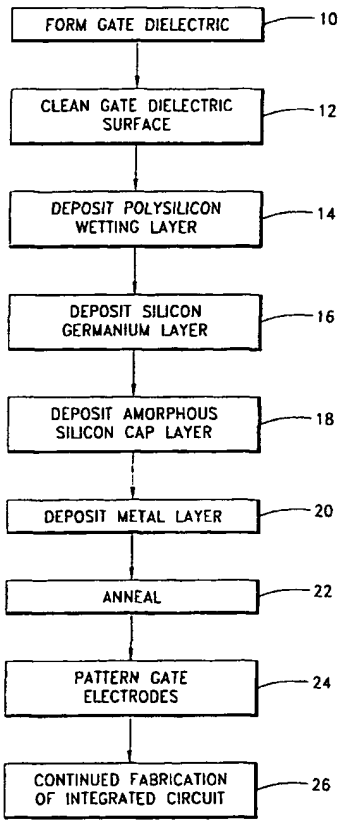
(54) Title: DEPOSITION OF GATE STACKS INCLUDING SILICON GERMANIUM LAYERS



(57) Abstract: Methods and structures are provided for forming silicon germanium gate electrodes over gate dielectrics. A thin polysilicon wetting layer (115) provides continuous coverage of the silicon dioxide layer (110) and reduces incubation time for the silicon germanium (120) thereupon. The continuity of the wetting layer (115) leads to a uniformly thick, planar gate electrode structure. At the same time, the polysilicon layer (115) can be made thin enough to minimize thermal requirements for segregating germanium to the electrode-oxide interface, and providing grain boundary diffusion to further facilitate germanium diffusion. Advantageously, the polysilicon wetting layer (115), silicon germanium (120) and a further silicon cap layer (125) are all formed in situ under atmospheric pressures.

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DEPOSITION OF GATE STACKS INCLUDING SILICON GERMANIUM LAYERS

Field of the Invention

The invention relates generally to the deposition of silicon-germanium layers, and more particularly to forming transistor gate electrodes including silicon-germanium.

Background of the Invention

Integrated circuit design is constantly being scaled down in pursuit of faster circuit operation and lower power consumption. Scaled dimensions in a circuit design generally requires attendant changes in fabrication processing.

A basic building block of integrated circuits is the thin film transistor (TFT). As is known in the art, the transistor typically includes a gate electrode separated from a semiconductor layer or substrate by a thin gate dielectric material. Although a common acronym for state-of-the-art transistors is MOS, for metal-oxide-silicon, the material of choice for the gate electrode has long been silicon rather than metal. Among other advantages, silicon gate electrodes are able to withstand high temperature processes and enable self-aligned doping processes used for completing the transistor, thus saving expensive masking steps. Many circuit designs often include more highly conductive strapping layers over the polysilicon gate electrode, to enhance lateral conductivity across the integrated circuit (e.g., where the upper portion of the gate electrode stack serves as a word line in a memory device). For example, metal can be deposited over a polysilicon gate electrode, and top portions of the polysilicon can be consumed in a heating step. The heating step causes a reaction of the deposited metal with the upper portions of the silicon, to form a metal silicide such as titanium silicide or tungsten silicide. In the process, a portion of the silicon is consumed.

Recently, interest has been drawn to the possibility of doping silicon electrodes with germanium, thereby reducing the electrical work function of the transistor gate electrode. Accordingly, a reduced voltage is needed to operate the circuit, consequently generating less heat. Moreover, a silicon germanium gate electrode remains compatible with surrounding materials and current integrated circuit fabrication processes.

Proposals for forming silicon germanium layers include in situ doping of a silicon layer by forming germane (GeH_4) along with silane (SiH_4) in a chemical vapor deposition process. While such in situ doped CVD processes have been found to be effective in producing silicon germanium, the addition of germane to the silane flow has been found to significantly reduce incubation times over dielectric materials such as silicon dioxide, leading to lower throughput and consequently greater fabrication costs. The semiconductor industry is very sensitive to fabrication costs. Accordingly, any increase in wafer throughput, at any stage of processing, translates to reduced production costs and higher margins.

Another concern in the semiconductor fabrication industry in general is that of maintaining low profiles and planarity from level to level. Poor step coverage and high profile features, particularly during front-end processing, tend to be amplified through higher levels of chip fabrication. Topographical anomalies raise problems for photolithographic steppers, risking misalignment in critical masking steps.

One manner of addressing such issues is to carefully control deposition processes to obtain uniform thickness and composition of deposited thin films. CVD, and particularly low pressure CVD (e.g., less than about 1 Torr), is therefore typically employed for deposition whenever possible. Advantageously, LPCVD also more efficiently deposits reactant gases, as compared to higher pressure processes, thus reducing operational costs. Unfortunately, greater uniformity of composition and conformality with LPCVD comes at the expense of lower deposition rates and therefore lower throughput.

Accordingly, a need exists for reducing the costs of depositing silicon germanium.

Summary of the Invention

1. In satisfaction of this need, methods are provided herein for forming gate stacks including silicon germanium with rapid incubation and high deposition rates. At the same time, the resultant gate stacks have very low surface roughness.

2. In accordance with one aspect of the invention, a method is described for forming a transistor gate electrode on a semiconductor substrate. The method includes depositing a polysilicon layer to a thickness between about 15 Å and 100 Å directly on a gate dielectric layer. A silicon germanium layer is then deposited directly on the polysilicon layer.

In accordance with another aspect of the invention, a process is provided for depositing a silicon germanium layer over a silicon-containing dielectric layer. The process includes depositing a polysilicon wetting layer over the dielectric. A silicon germanium layer is formed by chemical vapor deposition directly over the polysilicon. Germanium from the silicon germanium layer diffuses to an interface with the dielectric. In the process, each of the polysilicon and silicon germanium depositions is conducted at greater than about 500 Torr.

In accordance with another aspect of the invention, a method is provided for forming a transistor gate stack having a surface roughness of less than about 50 Å rms. The method includes forming a silicon oxide gate dielectric, depositing a silicon wetting layer and depositing a germanium-doped silicon layer. The wetting layer has a thickness between about 15 Å and 50 Å. The germanium-doped silicon layer is in situ doped and formed directly upon the silicon layer at greater than about 700 Torr.

3. Brief Description of the Drawings

These and other aspects of the invention will be readily apparent from the following description and from the appended drawings, which are meant to illustrate and not to limit the invention, and wherein:

FIGURE 1 is a flow chart generally illustrating the process of forming a gate stack in accordance with the preferred embodiment of the present invention;

FIGURE 2 illustrates a semiconductor substrate, representing the upper surface of a work piece in accordance with the preferred embodiment;

FIGURE 3 illustrates the substrate in Figure 2 after formation of a gate dielectric layer over the substrate surface;

FIGURE 4 illustrates a polysilicon wetting layer deposited directly over the gate dielectric layer of Figure 3;

FIGURE 5 illustrates a silicon germanium layer deposited directly over the polysilicon wetting layer of Figure 4;

FIGURE 6 illustrates continued deposition of a silicon layer over the silicon germanium layer of Figure 5;

FIGURE 7 illustrates a metal layer deposited over the silicon cap layer of Figure 6;

FIGURE 8 illustrates the product of an anneal step, siliciding the metal layer with the upper silicon portion of the gate electrode and segregating germanium at the gate electrode/dielectric interface;

FIGURE 9 is an auger profile of a continuous silicon germanium layer deposited by methods of the preferred embodiments over a silicon oxide layer;

FIGURE 10 is an auger profile of a discontinuous silicon germanium layer deposited on an amorphous silicon seed layer over a silicon dioxide film.

FIGURE 11 is a scanning electron micrograph (SEM) of a discontinuous silicon germanium layer deposited over an amorphous seed layer; and

FIGURE 12 is a transmission electron micrograph (TEM) of a continuous silicon germanium layer deposited over a polysilicon wetting layer on top of a silicon dioxide substrate, in accordance with the preferred embodiments.

Detailed Description of the Preferred Embodiment

The skilled artisan will readily appreciate that the principles disclosed herein will have application to a variety of contexts in which silicon germanium deposition is desired. Moreover, the principles disclosed herein will have application to other deposition processes in which seed layers are desired. The invention has particular utility, however, in forming transistor gate stacks.

With reference initially to Figure 1, a process in accordance with a preferred embodiment of the present invention is generally illustrated. As will be understood from the more detailed discussion below with respect to Figures 2 to 8, various omissions and modifications from the illustrated sequence can be made, depending upon the particular needs of the integrated circuit design in which a transistor gate stack is desired.

Initially, a gate dielectric is formed 10 over a semiconductor substrate. Preferably, the gate dielectric comprises silicon nitride or silicon oxide, for which integration techniques are well-developed. In accordance with state-of-the-art processing, the gate dielectric comprises a high quality silicon dioxide layer in the illustrated embodiment. Typically, such a gate dielectric is thermally grown from the surface of the underlying silicon substrate. The skilled artisan will readily appreciate a number of suitable processes and parameters for forming gate dielectrics. Moreover, many other materials are currently being investigated for replacement of silicon oxide as the gate dielectric, including materials exhibiting higher permittivity. The processes described herein will also have application to deposition over such alternative materials.

The surface of the gate dielectric is then preferably cleaned 12 to ensure purity of the in-process transistor. Preferably, a wet cleaning process comprises dipping or exposing the dielectric surface to dilute ammonium hydroxide and hydrogen peroxide in water to clean particle contamination from the oxide surface of the preferred gate dielectric. In the illustrated embodiment, the clean is a dilute SC1 clean, comprising a 1:2:100 concentration of $NH_4OH:H_2O_2:H_2O$

at about 35°C for 10 minutes, followed by about 6 minutes of de-ionized water rinse and a spin dry. The skilled artisan will readily appreciate other suitable processes for cleaning dielectric surfaces without excessive damage to the gate dielectric. Typically, the cleaning process is conducted outside a deposition chamber in which further processing will be conducted, although the wet cleaning tool may be mounted upon a cluster tool platform, such that exposure to contaminants is minimized between cleaning and deposition.

Following cleaning, the workpiece is loaded in a chemical vapor deposition chamber for deposition 14 of a polysilicon wetting layer. As set forth in more detail below, employment of polysilicon for this layer allows formation of a thin wetting layer while at the same time conserving thermal budgets and producing a smooth, uniformly thick gate stack.

Following deposition 14 of the polysilicon, a silicon germanium alloy, preferably having the form $Si_{1-x}Ge_x$, is deposited 16 over the polysilicon wetting layer. For simplicity, the silicon germanium layer will be referred to more generally as SiGe. Preferably, the SiGe deposition 16 immediately follows polysilicon deposition 14 within the same chamber. Thus, for example, the silicon source gas from the polysilicon deposition 14 can be continued or simply reduced while a germanium source gas, preferably germane (GeH_4), is added to the flow during chemical vapor deposition. More preferably, both polysilicon and poly-SiGe deposition are conducted under atmospheric or near-atmospheric conditions.

SiGe deposition 16 is followed by deposition 18 of a cap layer. The cap layer preferably comprises silicon, and most preferably amorphous silicon. A relatively thin cap layer (e.g., about 100 Å) can be employed to minimize the risk of oxidizing germanium in the SiGe layer. On the other hand, the cap layer may also serve as a sacrificial layer for later silicidation, in accordance with many gate stack designs. In this case, the cap layer is thicker and is preferably between about 1,000Å and 1,500Å.

In the illustrated embodiment, deposition of an amorphous silicon cap is followed by formation 20 of a metal layer over the cap layer. This metal layer can then be annealed 22 to react the overlying metal with the underlying silicon, in a standard silicidation reaction. While not illustrated, a dielectric cap layer can also be deposited over the conductive layers of the gate stack described above.

Once the gate stack has been completed, the gate electrodes are preferably patterned 24 by conventional photolithographic techniques and etching. In other arrangements, the gate electrodes can be patterned prior to deposition of the metal layer, and the metal can be employed in a self-aligned silicidation, as is known in the art.

Having completed the gate stack, further processing to complete the integrated circuit follows. For example, gate stacks typically are insulated by blanket deposition of a dielectric and spacer etch. Transistor active areas are then doped to form source and drain regions to either side of the patterned electrodes, and wiring or "back end" processes complete the circuit.

Reference is now made to Figures 2 to 8, illustrating the resultant structures after the preferred processes of Figure 1.

Referring initially to Figure 2, a semiconductor substrate 100 is provided on or in a workpiece. The semiconductor substrate 100 typically comprises an epitaxial silicon layer or the upper surface of a single-crystal, intrinsically doped silicon wafer, although the skilled artisan will appreciate that other semiconductor materials (e.g. III-V materials) can be substituted.

With reference now to Figure 3, a thin, conformal dielectric layer 110, preferably comprising silicon oxide or silicon nitride, is formed over the substrate 100. In the illustrated embodiment, the dielectric comprises a high quality thermal oxide grown from the semiconductor substrate 100. In accordance with present day circuit design, the gate dielectric 110 is preferably grown to a thickness of less than about 7 nm (70 Å), more preferably less than about 5 nm and in the illustrated embodiment is about 3.0 nm. The gate dielectric 110 can be formed by other methods, as will be appreciated by the skilled artisan. Dielectric materials for future generation device might include Ta_2O_5, BST, SBT, BT and other materials having higher dielectric constants. The processes described herein are also applicable to deposition of SiGe layers over such advanced materials.

Following formation of the gate dielectric 110, the workpiece is typically removed from the furnace, rapid thermal oxidation (RTO) tool or other process chamber in which the gate dielectric 110 is formed, and the surface is cleaned prior to insertion in a CVD chamber.

Referring now to Figure 4, a thin wetting or seed layer 115 is deposited directly over the cleaned surface of the gate dielectric 110. The deposition preferably takes place within a chemical vapor deposition chamber (CVD) chamber, and in the illustrated embodiment, the wetting layer 115 is formed in a single wafer process chamber initially available under the trade name Epsilon™ from ASM America of Phoenix, AZ. Other suitable deposition chambers can also be employed. Advantageously, the horizontal flow configuration and advanced heating control system of the Epsilon™ reactor enable rapid deposition of a conformal wetting layer 115 at atmospheric pressures.

The wetting layer 115 is characterized by provision of rapid incubation of the material deposited thereupon, as well as electrical and chemical compatibility with the overlying layer. Most preferably, the wetting layer 115 is substantially consumed by later processing, such that the layer is not present in the final structure.

The wetting layer 115 of the illustrated embodiment comprises a polycrystalline silicon layer, or polysilicon. Polysilicon is compatible with the SiGe layer to be deposited thereupon, provides rapid incubation of in situ Ge-doped silicon layers, and is readily consumed by the SiGe. In particular, the polycrystalline nature of the layer enables formation of a thin layer while providing complete coverage of the dielectric layer 110, as well as providing diffusion paths along grain boundaries of the polysilicon. The layer 115 is thus readily "consumed" by segregation of germanium to the dielectric interface.

Accordingly, the deposition temperatures at atmospheric pressures in the preferred single-substrate CVD reactor are greater than about 550°C, under which conditions CVD silicon is at least partially polycrystalline. At greater than 650°C in such a chamber silicon is generally completely polycrystalline. Preferably, however, the temperature in deposition is between about 600°C and 700°C, and more preferably between 600°C and 650°C. Under these conditions, the wetting layer 115 demonstrates a low surface roughness while demonstrating predominantly

polycrystalline characteristics. The skilled artisan can, of course, readily adapt the teachings herein to determine appropriate deposition conditions for different reactors to accomplish a similar balance between surface roughness and polycrystalline composition. For example, temperatures to achieve the same composition can be from 50°C to 75°C lower for batch systems, as compared to the preferred single-workpiece Epsilon™ reactor.

The deposition is preferably conducted at greater than about 500 Torr, more preferably at greater than about 700 Torr, and is most preferably conducted at about atmospheric pressure (760 Torr). Slight pressure differentials due to gas flows are of negligible effect. Advantageously, deposition under close to atmospheric conditions reduces or eliminates expensive pump down between processes, requires fewer parts and enhances deposition rates.

In the illustrated embodiment, a silicon source gas and a reducing agent react on the surface of the workpiece in a chemical vapor deposition (CVD) reaction. The silicon source can comprise, for example, monosilane, disilane, dichlorosilane, or trichlorosilane, while the reducing agent for pyrolizing silane-based compounds is typically hydrogen. Preferably, monosilane (SiH_4) flows at between about 10 sccm and 100 sccm, more preferably between about 20 sccm and 50 sccm, while hydrogen (H_2) flows at between about 10 slm and 50 slm, more preferably with about 20 slm H_2.

The wetting layer 115 is preferably thin enough to enable diffusion from a later-formed SiGe layer. Desirably, the wetting layer 115 is thin enough to permit such diffusion without separate annealing steps. Furthermore, too thick a wetting layer can dilute germanium content in the final structure. Accordingly, the polysilicon layer 115 is preferably less than about 200 Å, more preferably less than about 100 Å, and most preferably less than about 50 Å. On the other hand, the polysilicon layer 115 should also be thick enough to ensure full coverage of the surface of the gate dielectric 110 without discontinuities. Accordingly, the polysilicon layer 115 is preferably greater than about 15 Å and more preferably greater than about 30 Å.

Referring now to Figure 5, a silicon germanium (SiGe) layer 120 is deposited over the polysilicon wetting layer 115. As discussed in the Background section above, the addition of germanium to traditional polysilicon gate electrode structures lowers the device work function at the oxide-electrode interface, thereby reducing voltage and heat generation during operation. Most desirably, the gate material is close to the mid-gap of silicon, that is, close to 0.55 eV. Advantageously, employing SiGe allows tailoring the work function by altering the germanium content, while maintaining compatibility and ease of integration with surrounding materials and existing fabrication techniques.

Preferably, the SiGe layer is polycrystalline. Accordingly, the remainder of the present description employs the term "poly-SiGe" to describe the layer 120. Preferably, therefore, the deposition is performed under conditions to form poly-SiGe. Temperature ranges particularly influence the crystallinity of deposited silicon germanium. The preferred deposition conditions are discussed in more detail below. In other arrangements, the layer 120 can be deposited as amorphous SiGe and later crystallized in an in situ or ex situ anneal at an elevated temperature. Advantageously, however, depositing under conditions that directly form poly-SiGe enables a high germanium incorporation with better distribution throughout the deposited film, as compared to amorphous films. Furthermore, poly-SiGe can be deposited at relatively high rates.

The deposition of poly-SiGe preferably comprises flowing a silicon source gas, a germanium source gas and a reducing agent in a chemical vapor deposition process. In the illustrated embodiment, the silicon source gas comprises monosilane (SiH_4), the germanium source gas comprises dilute germane (1.5% GeH_4 in H_2), and the reducing agent comprises hydrogen (H_2). Preferably, the silane flow is increased relative to the preceding polysilicon deposition, and can be between 50 sccm and 500 sccm, more preferably between about 100 sccm and 400 sccm. The dilute germane (1.5% germane in hydrogen in the illustrated embodiment) is preferably found between 50 sccm and 5,000 sccm, more preferably between about 100 sccm and 1,000 sccm. The hydrogen flow is preferably between 5 slm and 50 slm, more preferably about 20 slm.

In the illustrated embodiment, without the aid of plasma or other supplemental energy sources, temperature during the deposition preferably is between about 500°C and 800°C, more preferably between about 550°C and 650°C, most preferably is at about 600°C ∀ 15°C. At the lower end of these ranges, poly-SiGe deposition is too slow for commercial applications. At the upper end of these ranges, on the other hand, germanium incorporation into the layer is reduced and surface roughness increases.

As noted with respect to the polysilicon deposition, the poly-SiGe deposition is preferably conducted at greater than about 500 Torr, more preferably at greater than about 700 Torr, and is most preferably conducted at about atmospheric pressure (760 Torr). Slight pressure differentials due to gas flows are of negligible effect. As will be appreciated by the skilled artisan, atmospheric deposition reduces the efficiency with which precursors are converted to deposited poly-SiGe. However, the inventor has found deposition under atmospheric pressures to attain greater benefits to operational efficiency, including the reduction or elimination of expensive evacuation steps between processes and particle contamination caused by pressure fluctuations. Additionally, atmospheric deposition entails lower capital costs by eliminating pumping equipment and chamber reinforcement for reduced pressure (1-200 Torr) and low pressure (less than 1 Torr) operation.

The germanium content in the poly-SiGe layer 120 is preferably between about 10% and 80%, more preferably between about 20% and 50%. The overall thickness of the layer is preferably between 500 Å and 1,500 Å, and more preferably between about 500 Å and 1,000 Å.

An exemplary recipe includes flow of about 500 sccm 1.5% germane, 100 sccm silane and 20 slm hydrogen at atmospheric pressure and 600°C. Such flows produce a silicon germanium layer with a germanium content of between about 18% and 20%. With the same hydrogen and silane flow, 4,500 sccm dilute germane silane produces a germanium content of about 50%.

Advantageously, the presence of a polysilicon wetting layer 115 enables rapid incubation and therefore faster deposition times for the poly-SiGe layer. Direct deposition of in situ germanium-doped silicon layers (without a wetting layer) tends to etch the underlying gate dielectric (particularly silicon oxide or silicon nitride) in competition with deposition, thus increasing incubation times. As will be appreciated by the skilled artisan, the increased incubation time and consequent increase in overall deposition time results in lower wafer throughput, which can mean

the difference between commercially viable and non-viable processes in the highly competitive semiconductor fabrication industry.

With reference to Figure 7, a cap layer 125 is preferably deposited directly over the poly-SiGe layer 120. In the illustrated embodiment, this cap layer 125 is deposited under the same atmospheric pressures in situ immediately following formation of the poly-SiGe layer, without removing the workpiece from the CVD chamber. Accordingly, the poly-SiGe layer 120 is not exposed to the clean room atmosphere and oxidation of germanium in the layer 120 is avoided. Accordingly, the cap layer 125 is preferably silicon, and more preferably comprises amorphous silicon. Amorphous silicon advantageously minimizes or slows diffusion of germanium through the cap layer 125.

The amorphous silicon cap layer 125 preferably has a thickness between about 100 Å and 1,500 Å. The lower end of this range is a sufficient thickness to achieve the sealing function of the cap layer 125. In the illustrated embodiment, however, the cap layer 125 can also serve as a silicon source for a later silicidation step. Accordingly, the illustrated cap layer 125 has a thickness of about 1,000 Å.

While in situ forming the cap layer 125 after the poly-SiGe layer 120, hydrogen and silane continue to flow, with silane preferably between about 100 sccm and 400 sccm, more preferably increased relative to the poly-SiGe deposition to about 200 sccm. As discussed above, deposition temperatures of less than about 550°C result in the desired amorphous structure for the preferred single-workpiece CVD tool.

The gate stack can then be completed by any of a number of conventional processing techniques. With reference to Figure 7, in the illustrated embodiment the workpiece is removed from the CVD chamber, and a highly conductive strapping layer is formed over the poly-SiGe layer 120 by first depositing a metal layer 150 (e.g., titanium or tungsten). The thickness of the metal layer 130 is selected to completely or partially react with the underlying cap layer 125, depending upon circuit design considerations. Preferably, a metal layer comprises tungsten or titanium and has a thickness between about 1,000 Å and 2,000 Å. As noted above with respect to Figure 1, this deposition can be conducted prior to or after patterning the electrodes.

With reference to Figure 8, the gate stack is shown after a conventional silicidation anneal. A metal silicide layer 155 results through partial or complete consumption of the sacrificial cap layer 125 (Figure 7). A residual metal layer and or metal nitride layer (not shown) can also overlie the silicide 155, depending upon the relative thicknesses of the cap layer 125 and metal layer 150. A further high temperature anneal can also be performed to re-orient the silicide crystals to a more highly conductive state.

During the course of higher temperature processing, such as the above-noted silicidation anneal, germanium in the deposited poly-SiGe layer 120 (Figure 7) diffuses downwardly through the thin polysilicon wetting layer 115 (Figure 7). Such diffusion is particularly facilitated by the thinness of the deposited wetting layer 115, and by the polycrystalline nature of that layer, even in the absence of a particular anneal step. Diffusion along grain boundaries spread throughout the polysilicon layer 115 is rapid, leading to a desired germanium concentration at a gate electrode-dielectric interface 160, where it is needed most in order to engineer and control the work-function. The thin

polysilicon wetting layer 115 (Figure 7) thus obviates any separate, time-consuming, high temperature anneal step to segregate germanium at the interface.

In view of the disclosures herein, the skilled artisan will readily appreciate that segregation of germanium through the wetting layer 115, consuming the wetting layer 115 and leaving a poly-SiGe electrode 150, can take place naturally during any thermal processing steps in the further fabrication of the integrated circuit. Thus, while illustrated as occurring during silicidation, germanium may have already diffused through to the electrode-oxide interface during deposition of the cap layer 125 or the metal layer 130. Alternatively, a separate anneal can be conducted, depending upon the thickness of the wetting layer and the presence or lack of further high temperature processing during subsequent fabrication processes.

Advantageously, the use of a polysilicon wetting layer in conjunction with the poly-SiGe layer ensures a continuous, planar layer across the dielectric surface. Planarity in the wetting layer 115 allows similarly planar layers to be deposited thereupon, such that the gate stack (including wetting layer, poly-SiGe layer and polysilicon cap layer) can be smooth. Preferably, the resultant gate stack has a surface roughness less than about 100 Å root mean square (rms), more preferably less than about 50 Å rms and most preferably less than about 20 Å rms. Planarity of the gate stack is important to achieving uniformity in later processes, particularly for scaled-down dimensions of state-of-the-art and future generation circuit designs.

Figures 9 and 10 graphically demonstrate the continuity of the wetting layer 115 and overlying poly-SiGe layer 120 when the wetting layer 115 comprises polysilicon. Figure 9 is an Auger profile of a wetting layer and poly-SiGe layer (prior to anneal), constructed in accordance with the preferred embodiment. The atomic composition of the layers is analyzed as electrons bombard the workpiece, such that the left side of the chart represents the topmost surface of the poly-SiGe/polysilicon bilayer, while the right side represents depth into the layer. At a depth of around 1,400 Å, a sharp interface can be seen between the polysilicon layer and the underlying silicon oxide layer, where the silicon content sharply drops while the oxygen content sharply increases.

Figure 10 is an Auger profile of a poly-SiGe layer formed over an amorphous silicon wetting layer. Amorphous silicon is typically associated with smooth layers, and furthermore can be deposited at lower temperatures than polysilicon. In contrast to the profile of Figure 9, however, Figure 10 shows oxygen content throughout the electron bombardment process. This indicates a discontinuous wetting layer, which in turn propagates upwardly into the deposited poly-SiGe layer. Surface mobility of the amorphous silicon results in nodules or islands forming on the silicon oxide surface during deposition. The subsequent deposition of poly-SiGe layer incubates preferentially upon these nodules, while an etching reaction competes with deposition on the bare silicon oxide. Germanium atoms also demonstrate high surface mobility, tending to aggregate at the silicon nodules. Accordingly, the poly-SiGe layer is also "bumpy" and discontinuous, and the roughness is propagated into higher layers. The resultant rough gate stack would further complicate integration during later fabrication steps.

Figure 11 is a scanning electron micrograph (SEM) showing the surface of a poly-SiGe layer deposited on an amorphous silicon wetting layer over a silicon oxide substrate. The roughness or nodular appearance of the poly-SiGe surface is due to discontinuity in the underlying wetting layer.

Figure 12, on the other hand, shows a planar, smooth poly-SiGe layer directly over the silicon dioxide substrate. While the illustrated silicon dioxide substrate is much thicker than the typical gate dielectric, for purposes of the present description the silicon dioxide surface behaves identically to a thinner gate dielectric layer.

Referring again to Figures 7-8, the smoothness of the resultant poly-SiGe gate electrode layer 155 results from the consumed continuous polysilicon wetting layer 115 (Figures 4-7). Advantageously, polysilicon can be deposited in a very thin layer without compromising complete coverage of the dielectric layer 110. Desirably, a thin wetting layer 115 enables germanium diffusion therethrough to the interface with the gate dielectric 110. The polysilicon wetting layer 115 of the illustrated embodiment is particularly advantageous in that regard, as germanium diffusion is facilitated by grain boundaries in the polycrystalline material.

It will be appreciated by those skilled in the art that various omissions, additions and modifications may be made to the processes described above without departing from the scope of the invention, and all such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

I CLAIM:

4. 1. A method of forming a transistor gate electrode on a semiconductor substrate, comprising:

depositing a polysilicon layer having a thickness between about 15 Å and 100 Å directly on a gate dielectric layer; and

depositing a silicon germanium layer directly on the polysilicon layer.

2. The method of Claim 1, further comprising segregating germanium at an interface with the gate dielectric layer.

3. The method of Claim 2, wherein germanium from the silicon germanium layer diffuses through the polysilicon layer to the interface without a separate anneal step.

4. The method of Claim 2, wherein a germanium content at the interface with the gate dielectric layer is between about 20% and 50%.

5. The method of Claim 1, wherein depositing the polysilicon layer and depositing the silicon germanium layer are conducted in situ within one chemical vapor deposition chamber.

6. The method of Claim 1, wherein the polysilicon layer is deposited to a thickness of between about 30 Å and 50 Å.

7. The method of Claim 1, wherein depositing the silicon germanium layer comprises simultaneously flowing a silicon source gas and germane.

8. The method of Claim 1, further comprising depositing a cap layer over the silicon germanium layer.

9. The method of Claim 8, wherein the cap layer comprises amorphous silicon.

10. The method of Claim 9, wherein depositing the polysilicon layer, depositing the silicon germanium layer and depositing the cap layer are conducted in situ within one chemical vapor deposition chamber.

11. The method of Claim 9, further comprising depositing a metal layer over the cap layer and reacting the metal layer with the cap layer.

12. The method of Claim 1, wherein depositing the polysilicon layer comprises maintaining a substrate temperature between about 600°C and 700°C.

13. The method of Claim 12, wherein depositing the polysilicon layer comprises maintaining a substrate temperature between about 600°C and 650°C.

14. The method of Claim 1, wherein the gate stack has a surface roughness of less than about 50 Å rms.

15. The method of Claim 14, wherein the gate stack has a surface roughness of less than about 20 Å rms.

16. The method of Claim 1, wherein depositing the silicon germanium layer comprises a chemical vapor deposition at greater than about 500 Torr.

17. The method of Claim 16, wherein depositing the silicon germanium layer comprises a chemical vapor deposition at about atmospheric pressures.

18. The method of Claim 1, wherein the gate dielectric layer comprises silicon dioxide.

19. A process of depositing a silicon germanium layer over a silicon-containing dielectric layer, the process comprising depositing a polysilicon wetting layer over the dielectric layer, chemical vapor depositing the silicon germanium layer directly over the polysilicon, and diffusing germanium from the silicon germanium layer to an interface with the dielectric layer, wherein depositing each of the polysilicon and silicon germanium layers is conducted at greater than about 500 Torr.

20. The process of Claim 19, wherein the dielectric layer comprises silicon dioxide.

21. The process of Claim 19, wherein the dielectric layer comprises silicon nitride.

22. The process of Claim 19, wherein chemical vapor depositing the silicon germanium layer comprises simultaneously flowing a silane-based silicon source gas and germane.

23. The process of Claim 19, wherein depositing the polysilicon wetting layer comprises maintaining a deposition temperature of between about 600°C and 700°C in a single-substrate deposition chamber.

24. The process of Claim 23, wherein depositing the polysilicon wetting layer comprises maintaining a single substrate deposition chamber at about atmospheric pressure.

25. The process of Claim 19, wherein the polysilicon layer is deposited to a thickness between about 15 Å and 100 Å.

26. The process of Claim 25, wherein the polysilicon layer is deposited to a thickness between about 30 Å and 50 Å.

27. The process of Claim 26, wherein the dielectric layer comprises a gate dielectric over a semiconductor substrate.

28. A method of forming a transistor gate stack having a surface roughness of less than about 50 Å rms, the method comprising:

forming a silicon oxide gate dielectric;

depositing a silicon wetting layer having a thickness between about 15 Å and 50 Å; and

depositing an in situ germanium-doped silicon layer directly upon the silicon layer at greater than about 700 Torr.

29. The method of Claim 28, wherein depositing the silicon layer comprises deposition conditions for forming a predominantly polycrystalline silicon material.

30. The method of Claim 29, wherein depositing the silicon layer comprises maintaining a deposition temperature of between about 600°C and 700°C in a single-substrate chemical vapor deposition chamber.

31. The method of Claim 28, further comprising depositing an amorphous silicon cap layer over the germanium-doped silicon layer.

32. The method of Claim 31, wherein the silicon wetting layer, the germanium-doped silicon layer and the amorphous silicon cap layer are all deposited in situ under about atmospheric pressures within a single-substrate deposition chamber.

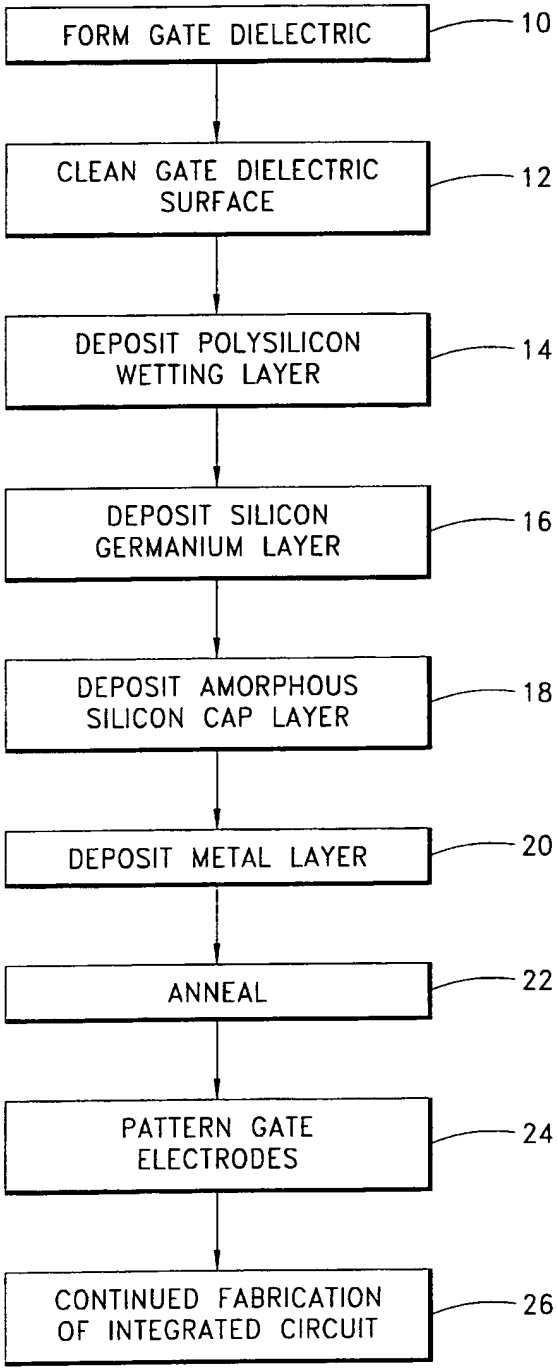

FORM GATE DIELECTRIC
10
CLEAN GATE DIELECTRIC SURFACE
12
DEPOSIT POLYSILICON WETTING LAYER
14
DEPOSIT SILICON GERMANIUM LAYER
16
DEPOSIT AMORPHOUS SILICON CAP LAYER
18
DEPOSIT METAL LAYER
20
ANNEAL
22
PATTERN GATE ELECTRODES
24
CONTINUED FABRICATION OF INTEGRATED CIRCUIT
26

Fig. 1

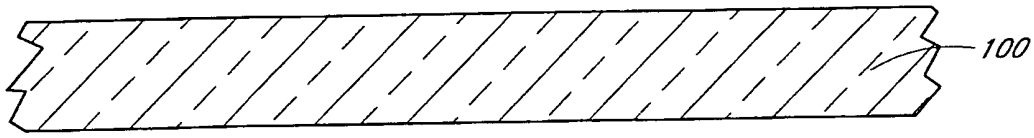


Fig. 2

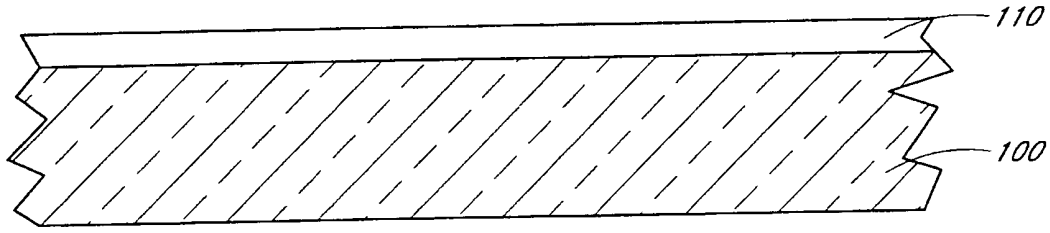


Fig. 3

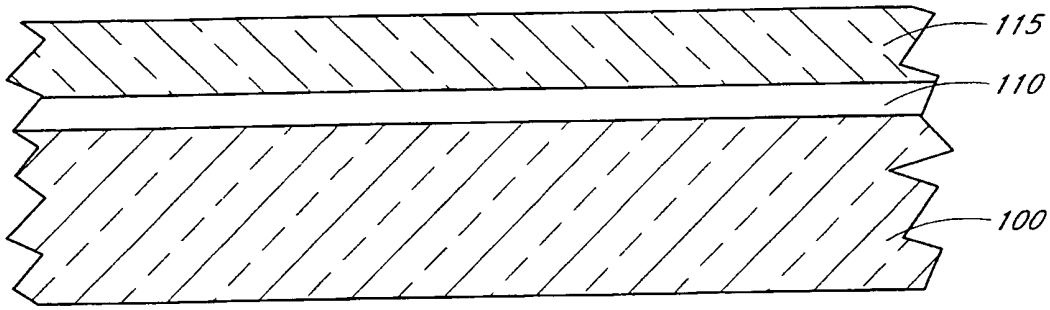


Fig. 4

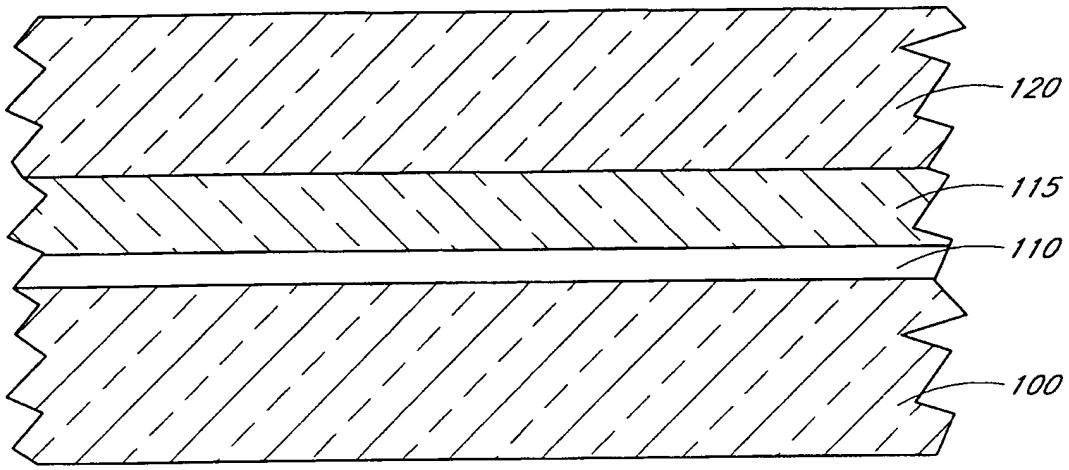


Fig. 5

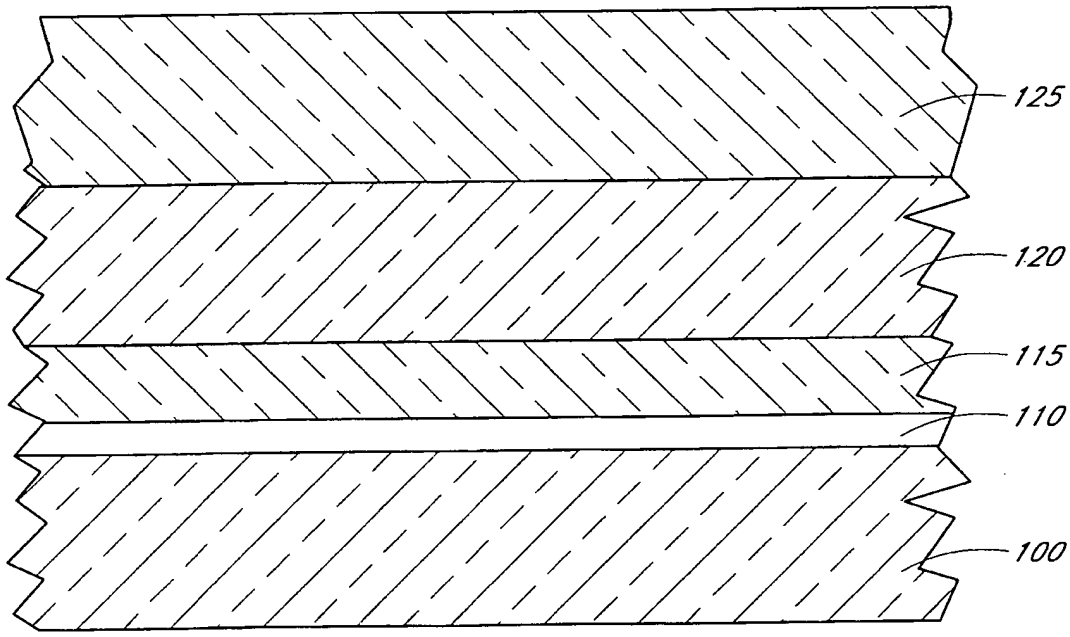


Fig. 6

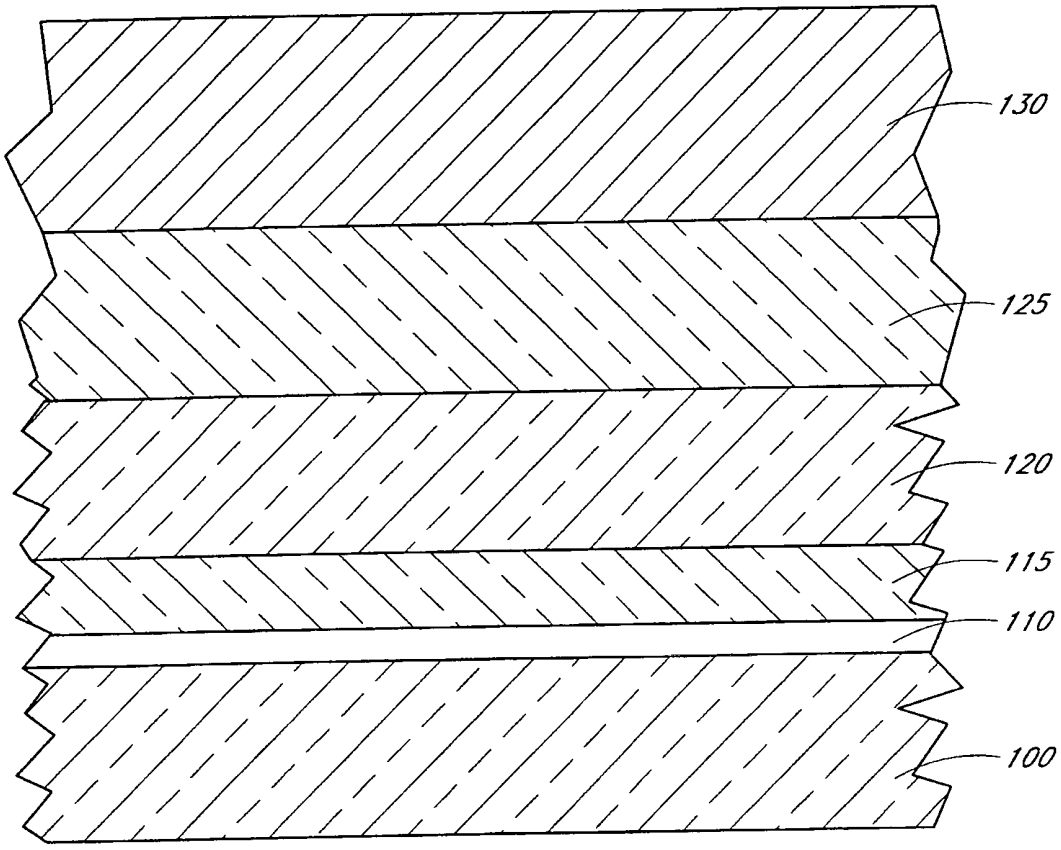
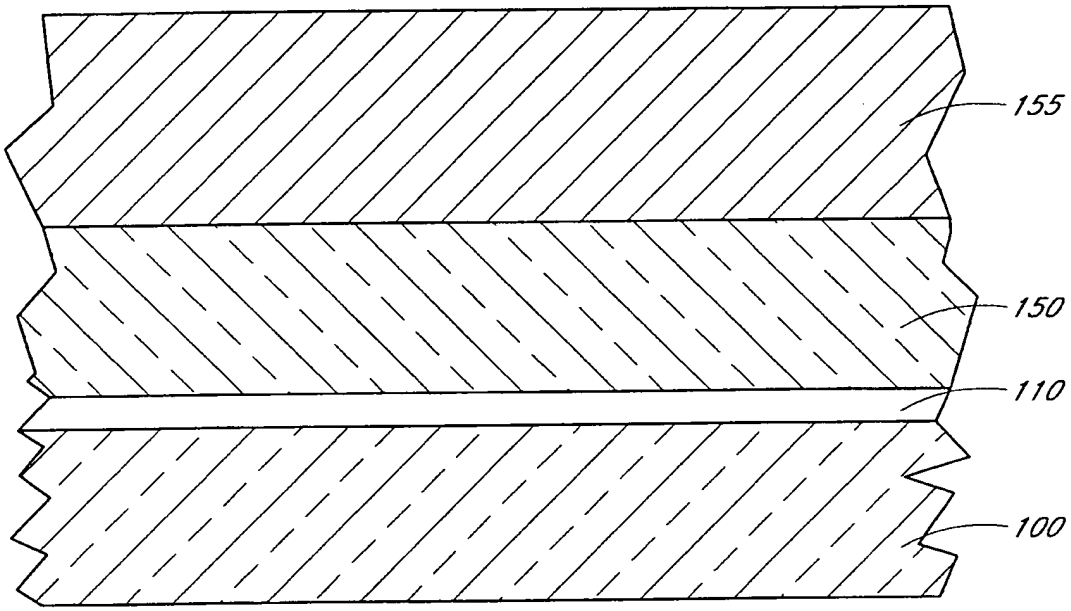


Fig. 7



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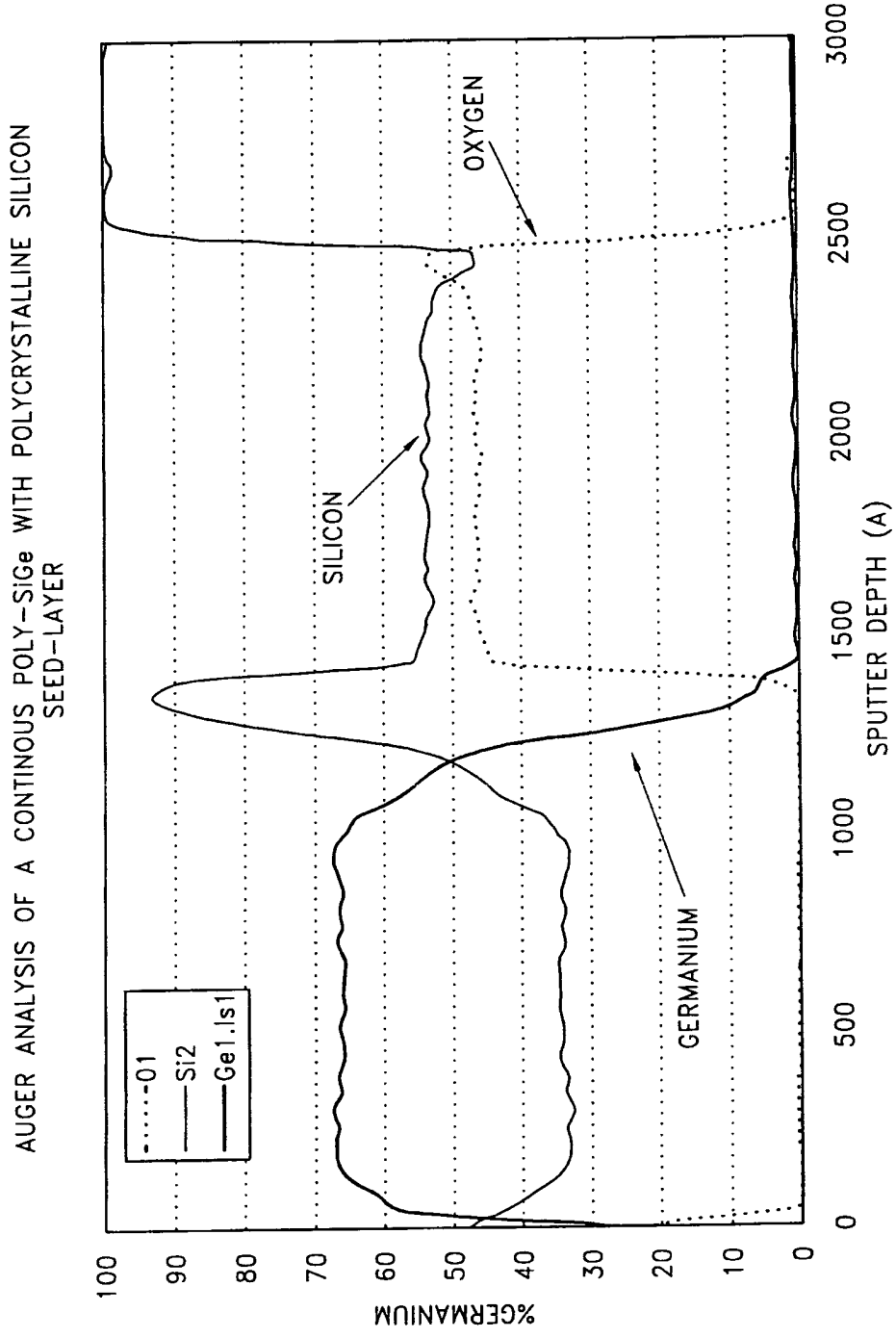
AUGER ANALYSIS OF A CONTINOUS POLY-SiGe WITH POLYCRYSTALLINE SILICON SEED-LAYER
-01
Si2
Ge1.ls1
SILICON
OXYGEN
GERMANIUM
%GERMANIUM
SPUTTER DEPTH (A)
0
10
20
30
40
50
60
70
80
90
100
0
500
1000
1500
2000
2500
3000

Fig. 9

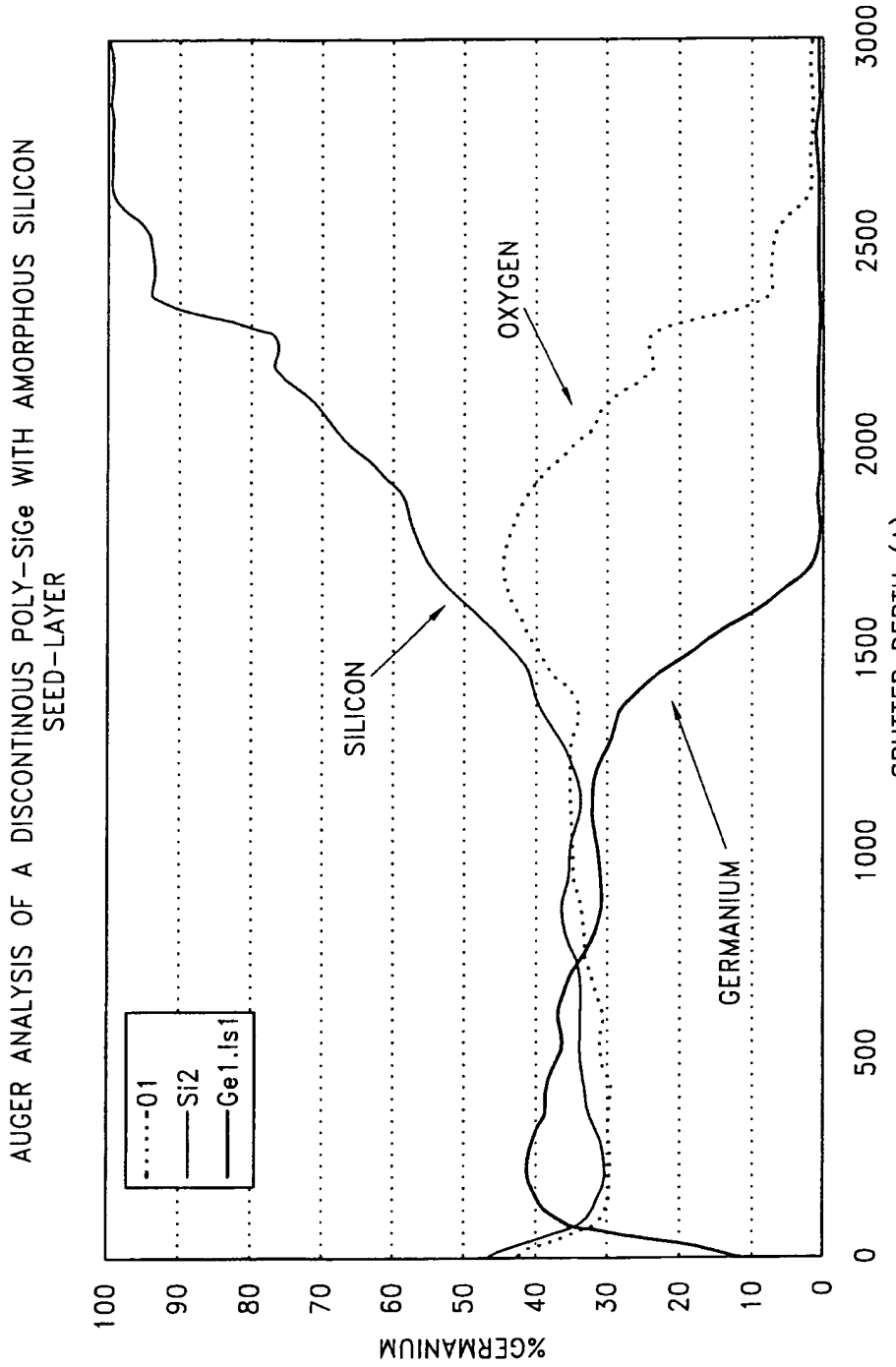
AUGER ANALYSIS OF A DISCONTINOUS POLY-SiGe WITH AMORPHOUS SILICON SEED-LAYER
-01
Si2
Ge1.Is1
SILICON
OXYGEN
GERMANIUM
%GERMANIUM
SPUTTER DEPTH (A)
0
10
20
30
40
50
60
70
80
90
100
0
500
1000
1500
2000
2500
3000

Fig. 10

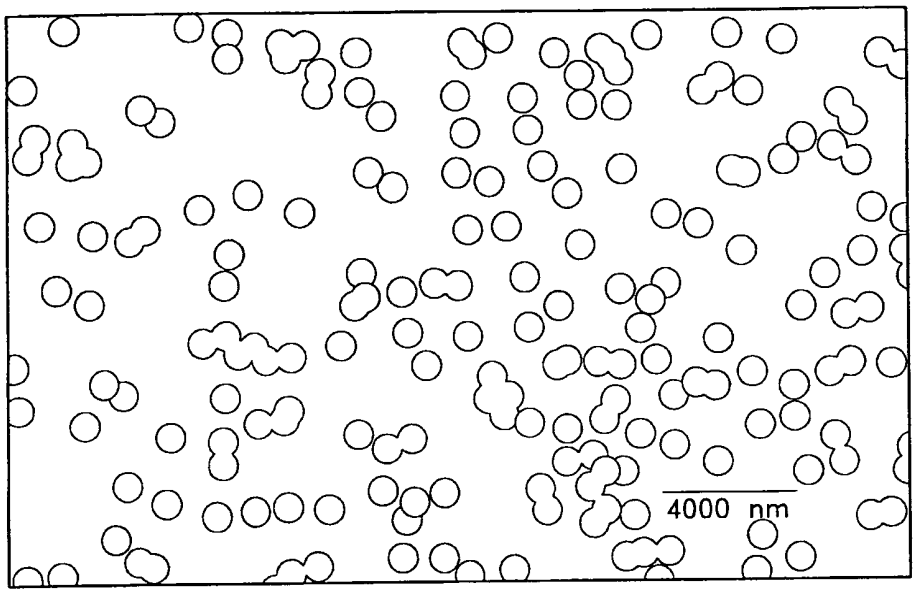

Fig. 11

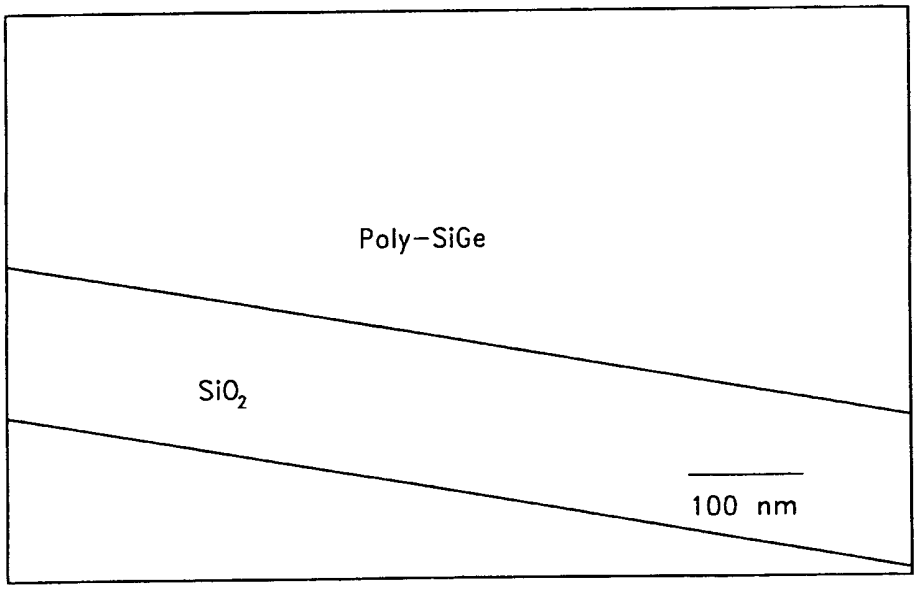

Fig. 12